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What is claimed is:

- 1 1. A method comprising:
2 amplifying data signals from a memory bus;
3 sampling the amplified data signals; and
4 selectively disabling the amplification in response to the absence of a
5 predetermined operation occurring over the memory bus.
- 1 2. The method of claim 1, wherein the selectively disabling comprises:
2 selectively disabling sense amplifiers.
- 1 3. The method of claim 1, wherein the selectively disabling comprises:
2 selectively disabling the amplification in response to the end of a particular
3 predetermined operation.
- 1 4. The method of claim 1, further comprising:
2 reading a data strobe signal from the bus;
3 delaying the data strobe signal; and
4 synchronizing the disablement of the amplification to an edge of the delayed data
5 strobe signal.
- 1 5. The method of claim 1, further comprising:
2 communicating signals associated with a double data rate memory device over the
3 memory bus.
- 1 6. The method of claim 1, wherein the predetermined operation comprises a
2 read operation.

1 7. The method of claim 1, wherein the predetermined operation comprises a
2 write operation.

1 8. A method comprising:
2 amplifying data signals from a memory bus;
3 sampling the amplified data signals; and
4 selectively enabling the amplification in response to a predetermined operation
5 occurring over the memory bus.

1 9. The method of claim 8, wherein the selectively enabling comprises:
2 selectively enabling sense amplifiers.

1 10. The method of claim 8, wherein the selectively enabling comprises:
2 selectively enabling the amplification in response to the beginning of the
3 predetermined operation.

1 11. The method of claim 8, further comprising:
2 synchronizing the enablement to the edge of a data strobe signal that appears on
3 the memory bus in connection with the predetermined operation.

1 12. The method of claim 8, further comprising:
2 communicating signals associated with a double data rate memory device over the
3 memory bus.

1 13. The method of claim 8, wherein the predetermined operation comprises a
2 read operation.

1 14. The method of claim 8, wherein the predetermined operation comprises a
2 write operation.

1 15. An apparatus comprising:
2 amplifiers to amplify data signals received from a memory bus;
3 a first circuit coupled to the amplifiers to sample the amplified data signals; and
4 a second circuit to selectively disable the amplifiers in response to the absence of
5 a predetermined operation occurring over the memory bus.

1 16. The apparatus of claim 15, wherein the second circuit selectively disables
2 the amplifiers in response to the end of a particular read operation.

1 17. The apparatus of claim 15, wherein the predetermined operation comprises
2 a read operation.

1 18. The apparatus of claim 15, wherein the predetermined operation comprises
2 a write operation.

1 19. The apparatus of claim 15, wherein the apparatus comprises a memory
2 controller.

1 20. The apparatus of claim 15, wherein the apparatus comprises a memory
2 device.

1 21. An apparatus comprising:
 2 amplifiers to amplify data signals received from a memory bus;
 3 a first circuit coupled to the amplifiers to sample the amplified data signals; and
 4 a second circuit to selectively enable the amplifiers in response to the
 5 predetermined operation occurring over the memory bus.

1 22. The apparatus of claim 21, wherein the second circuit selectively disables
 2 the amplifiers in response to the end of a particular read operation.

1 23. The apparatus of claim 21, wherein the predetermined operation comprises
 2 a read operation.

1 24. The apparatus of claim 21, wherein the predetermined operation comprises
 2 a write operation.

1 25. The apparatus of claim 21, wherein the apparatus comprises a memory
 2 controller.

1 26. The apparatus of claim 21, wherein the apparatus comprises a memory
 2 device.

1 27. A computer system comprising:
 2 a memory;
 3 a memory bus coupled to the memory;
 4 a processor to initiate a predetermined operation with the memory over the
 5 memory bus;
 6 amplifiers to amplify data signals received from the memory bus;
 7 a first circuit coupled to the amplifiers to sample the amplified data signals; and
 8 a second circuit to selectively disable the amplifiers in response to the absence of
 9 the predetermined operation occurring over the memory bus.

1 28. The computer system of claim 27, wherein the predetermined operation
 2 comprises one of a read operation and a write operation.

1 29. A computer system comprising:
 2 a memory;
 3 a memory bus coupled to the memory;
 4 a processor to initiate a predefined operation with the memory over the memory
 5 bus;
 6 amplifiers to amplify data signals received from the memory bus;
 7 a first circuit coupled to the amplifiers to sample the amplified data signals; and
 8 a second circuit to selectively enable the amplifiers in response to the
 9 predetermined operation occurring over the memory bus.

1 30. The computer system of claim 29, wherein the predetermined operation
 2 comprises one of a read operation and a write operation.